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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/625,285	07/22/2003	Peter R. Munguia	P16384	7500

25694 7590 10/03/2005

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EXAMINER	
DOAN, DUC T	
ART UNIT	**PAPER NUMBER**
2188	

DATE MAILED: 10/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/625,285	MUNGUIA ET AL.	
	Examiner	Art Unit	
	Duc T. Doan	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/7/05 3/25/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Status of Claims

Claims 1-23 are in the application.

Claims 1-23 are rejected.

Specifications

The disclosure is objected to because of the following informalities:

In Fig 1, block 118, it seem the label should be "Non volatile Memory".

Page 8, table 1, it is unclear the meaning of the cts in the header "encoded chip sel cts".

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

A person shall be entitled to a patent unless -

(a) the invention was known or used by other's in this country or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in a patent granted on an application for patent by another fled in the United States before the invention thereof by the applicant for patent, or on an international application by another

who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 1-23 is rejected under 35 U.S.C. 102 (b) as being anticipated by William et al (US 6199151).

As for claim 1, the claim recites an apparatus comprising a configuration store to select between an encoded chip select mode and an unencoded chip select mode, and an address decoder to generate unencoded chip select words in response to the unencoded chip select mode and to generate encoded chip select words in response to the encoded chip select mode. Williams describes an address decode (Fig 2) capable of generate "unencoded" chip select and "encoded" chip select (William's column 5 line 55 to column 6 line 6; Fig 3). William further suggests a flexibility to use either encoded or unencoded chip select in column 6 lines 12-26. Thus it is inherently to have a register to indicate using either encoded or unencoded chip select.

As for claim 2, the claim recites wherein the address decoder in response to an address for a boot code nub generates a chip select word that selects the same memory device regardless of operating in the unencoded chip select mode or the encoded chip select mode. Conventionally, the address range for the boot code is assigned from 0 to 1Mbyte. Therefore, it's inherently to assign the addresses of the boot code to a fix memory device regardless of chip select mode.

As for claim 3, the claim recites wherein the address decoder in response to an address for a boot code nub generates an encoded chip select word that selects a predetermined memory device that comprises the boot code nub when in the encoded chip select mode, and generates an unencoded chip select that selects the predetermined memory device that comprises the boot

code nub when in the unencoded chip select mode (William's column 6 lines 27-50 describes the generation of chip select).

As for claim 4, the claim recites wherein the address decoder, in response to an address for a boot code nub, generates the unencoded chip select word for the address such that the unencoded chip select word comprises the encoded chip select word for the address. William describes when a TLB miss occurs; a new physical address is compared with configuration registers to determine the corresponding chip select (William's column 5, lines 35-57; Examiner notes that one activate chip select and seven inactivated chip selects value is corresponding to the claim's unencoded chip select word). This value is further encoded (8:3 encode) and stored in TBL for subsequence usage (Williams's column 6 lines 12-25).

As for claim 5, the claim recites wherein the address decoder, in response to an address for a boot code nub, generates the encoded chip select word for the address such that the encoded chip select word comprises exactly one active chip select bit, and generates the unencoded chip select word for the address such that the unencoded chip select word comprises exactly one active chip select bit. (See William's Fig 3 second row).

As for claim 6, William describes wherein the address decoder, in response to an address for a boot code nub, generates the encoded chip select word for the address such that the encoded chip select word comprises exactly one active chip select bit that corresponds to a predetermined chip select line used to select a memory device comprising the boot code nub (William's Fig 3 second row, encoded row value), and generates the unencoded chip select word for the address such that the unencoded chip select word comprises exactly one active chip select bit that corresponds to the predetermined chip select line William's Fig 3 second row, chip select) .

William further describes the value in Fig 3 corresponds to values "predetermined" and kept in the TLB (William's column 4 line 60 to column 5 line 12).

As for claim 7, the claim recites wherein the address decoder, in response to an address for a boot code nub, generates the encoded chip select word such that a lowest order bit of the encoded chip select word is the only active bit of the encoded chip select word, and generates the unencoded chip select word such that a lowest order bit of the unencoded chip select word is the only active bit of the unencoded chip select word. It's rejected based on the same rationale as in the rejection of claim 5. Although in William's Fig 3 the encoded row value start from 0,1, to 7. It would be an obvious modification that the encoded row value to start from 1,2..7 to 0. William has anticipated some variation in the encoding implementation by the teaching found in column 5 line 65 to column 6 line 7; column 6 lines 14-26).

Claim 8 rejected base on the same rationale as in the rejection of claim 1.

Claim 9 rejected base on the same rationale as in the rejection of claim 3.

As for claim 10, William describes a chip select decoder coupled to the apparatus and coupled to each of the memory devices of the plurality of memory devices via a separate chip select line, wherein the chip select decoder activates the chip select line of the memory device with the boot code nub in response to receiving the encoded chip select word for the address from the apparatus (William's Fig 2 #57).

Claim 11 rejected base on the same rationale as in the rejection of claim 2.

Claim 12 rejected base on the same rationale as in the rejection of claim 4.

Claim 13 rejected base on the same rationale as in the rejection of claims 3 and 5.

As for claim 14, the claim recites updating an operation mode to one of the encoded chip select mode and the unencoded chip select mode. William further suggests a flexibility to use either encoded or unencoded chip select in column 6 lines 12-26.

As for claim 15, the claim recites executing the boot code nub, updating an operation mode to the encoded chip select mode in response to executing the boot code nub, and reassigning chip select pins not used to carry encoded chip select words after updating the operation mode. William describes the boot code must be executed first before the processor can do subsequent steps such as generating memory mapping of devices (William's column 5 lines 40-45). Therefore selecting or switching encoding modes for chip select should be done only "in response" to executing the boot code.

As for claim 16 the claim recites executing the boot code nub, updating an operation mode to the encoded chip select mode in response to executing the boot code nub, and reassigning chip select pins not used to carry encoded chip select words after updating the operation mode. The claim rejected based on the same rationale as in the rejection of claim 15. William further describes generating a map of devices (William's column 5 lines 40-45 and using page mapping for lookup tables in column 5 lines 1-10).

Claims 17-18,21-22 rejected base on the same rationale as in the rejection of claim 6.

Claim 19,27 rejected base on the same rationale as in the rejection of claim 7.

As for claim 20, the claim recites generating, in response to an address of a boot code nub and an encoded chip select mode, an encoded chip select word that selects a memory device with the boot code nub, and generating, in response to the address of the boot code nub and an unencoded chip select mode, an unencoded chip select word that comprises the encoded chip

select word of the boot code nub. The claim rejected based on the same rationale as in the rejection of claim 1. William describes the chip select (Fig 2: #57 cs1-cs8) generated from encoded row value (Fig 2: #59).

Claim 23 rejected base on the same rationale as in the rejection of claim 7.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

When responding to the office action, Applicant is advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Duc T. Doan whose telephone number is 571-272-4171. The examiner can normally be reached on M-F 8:00 AM 05:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 571-272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kevin L. Ellis
Primary Examiner